CLAIMS

What is claimed is:

1. A method of fabricating a semiconductor chip for direct attachment to a carrier, comprising:

providing a partially manufactured chip having a top surface;

applying a metal layer over said top surface of said chip;

applying a passivation layer over said metal layer;

selectively removing portions of said passivation layer to create one or more openings exposing portions of said metal layer;

forming solderable metal contact regions on said one or more openings;

wherein said solderable metal contact regions electrically connect to said carrier when said chip is positioned face down on said carrier, supplied with a thin layer of solder and heated.

2. The method as in claim 1 wherein said one or more solderable metal contact regions is made of materials selected from the group consisting of a TiCu metal layer combination, a TiNiAg metal layer combination and an AlNiVCu metal layer combination.

3. The method as in claim 1 wherein said metal layer is aluminum.

4. The method as in claim 1 wherein said one or more solderable metal contact regions are approximately 1 μm thick.

5. A semiconductor chip for directly connecting to a carrier, comprising:

a metal layer applied to a top surface of said chip;

a passivation layer applied over said metal layer such that portions of said passivation layer is selectively removed to create one or more openings exposing portions of said metal layer;

one or more solderable metal contact regions formed on each of said one or more openings; wherein said solderable metal contact regions electrically connect to said carrier when said chip is positioned face down on said carrier, supplied with a thin layer of solder and heated.

6. The chip as in claim 5 wherein said one or more solderable metal contact regions is made of materials selected from the group consisting of a TiCu metal layer combination, a TiNiAg metal layer combination and an AlNiVCu metal layer combination.

7. The chip as in claim 5 wherein said metal layer is aluminum.

8. The chip as in claim 5 wherein said one or more solderable metal contact regions are approximately 1 μm thick.

9. A Lateral Discrete Power Semiconductor MosFET Comprising:

(a) a semiconductor substrate;

(b) at least one first doped region in said semiconductor substrate forming at least one source;

(c) at least one secomd doped region in said semiconductor substrate forming at least one drain;

(d) a first connectivity layer at least one first runner and at least one second runner, wherein said at least one first runner is operatively connected to said at least one first doped region and said at least one second runner is operatively connected to said at least one second doped region.

(e) A second connectively layer operatively connected to said first connectively layer and having at least one third runner and at least one forth runner, wherein said at least one third runner is operatively connected to said at least one fourth runner is operatively connected to said at least one second runner.

(f) A third connectively layer having at least one first pad operatively connected to said at least one third runner and at least one second pad operatively connected to sid at least one fourth runner.

10. A semiconductor device of claim 9 wherein said at least one pad has at least pne first copper pillar or one metal layer and said at least one first pad said at least one second pad arranged in s substantially checker board pattern.

11. A semiconductor device of claim 10 wherein said at least one first pad is interleaved with said at least one second pad.

12. A semiconductor device of claim 9 wherein said at least one first doped region is a source for transistor and said at least one second doped region is a drain for a transistor

13. A semiconductor device of claim 12 wherein said at least one source and at least one drain are laid out susbstantially elongated shape and wherein said at least one source are interleaved with said at least one drain.

14. A semiconductor device of Claim 12 wherein said at least one source and at least one drain are laid out in substantially checkerboard pattern.

15. A Lateral discrete Power MosFET device comprising:

(a) semiconductor substrate

(b) at least one first doped region in said semiconductor substrate forming at least one source:

(c) at least one second doped region in said semiconductor substrate forming at least one drain:

(d) a first connectivity layer operatively connected to said first connectively layer and operatively connected to said at least one second doped region.

16 A Lateral discrete power semiconductor device of claim 15 wherein said second conductivity layer is operatively connected to said st least one second doped region through said first conductivity layer

17 A lateral discrete power semiconductor device of claim 16 wherein said second conductivity layer is operatively connected to said at least one second doped region through said first conductivity layer and using a portion of said first conductivity layer for such connection.

18 A lateral discrete power semiconductor device of claim 15 having a third conductivity layer with at least one first pad and at least on second pad of such layer wherein said at least one first pad is operatively connected to said first connectiveity and said at least one second pad is operatively connected to said second connectivity layer.

19 A Lateral discrete power semiconductor of claim 18 wherein said at least one first pad has at least one first copper pillar bump or copper direct attach or solder bump and at least one second pad has at least one second copper pillar bump or copper direct attach or solder bump.

20 A lateral discrete Power semiconductor of claim 19 wherein at least one first pad and said at least one second pad are arranged in a substantially checkerboard pattern.

21 A lateral discrete Power semiconductor of claim 19 wherein at least one first pad is interleaved with said at least one second pad.

22 A lateral discrete Power Semiconductor of Claim 15 wherein said at least one source at least one drain are laid out in substantially elongated shape and wherein said at least one source are interleaved with said at least one drain.

23 lateral discrete Power Semiconductor of Claim 15 wherein said at least one source at least one drain are laid out in substantially checkerboard pattern

24 A Lateral discrete Power MosFET device comprising:

(a) semiconductor substrate

(b)at least one first doped region in said semiconductor substrate forming at least one source:

(c)at least one second doped region in said semiconductor substrate forming at least one drain:

(d)a first connectivity having at least one first runner operatively connected to said at least one first doped region and at least one second runner operatively connected to at least one second runner operatively connected tosaid at least one second doped region:

(e) a second connectivity layer having at least one first pad operatively connected to said at least one first runner and at least one second pad operatively connected to said ay least one second runner.

25 A Lateral discrete Power MosFET of Claim 24 wherein said at least one copper pillar bump or one copper direct die attach or one solder bump and said at least one second pad has at ;east one second copper pillar bump or copper direct die attach or one solder bump

26 A Lateral discrete Power MosFET of Claim 25 wherein said at least one first pad and said at least one second pad are arranged in a substantially checkerboard pattern.

27 A Lateral discrete Power MosFET of Claim 25 wherein said at least one first pad is interleaved with said at least one second pad.

28 A Lateral discrete Power MosFET of Claim 24 wherein said at least one source and at least on edrain are laid out in substantially elongated shape and wherein said at least on esorce are interleaved with said at least one drain.

29 A Lateral discrete Power MosFET of Claim 24 wherein said at least one source and at least on edrain are laid out in substantially checkerboard pattern

30 The combination of a Lateral discrete Power MosFET using source and drain regions arranged in three metal system with the first metal that is in contact with the silicon surface arranged in a checker board pattern , followed by two additional striped metal structures to bring the source, drain and gates to the

corresponding copper pillar bumps. The Source and Drain Regions of the planar Mosfet are parallel stripes both with 90 degree angle between Metal 1 and Metal 2 and the third layer is 500um square pads.